REMARKS

Status of Claims

Claims 1-5, 7 and 8 were pending at the time of the Office action. Claims 1-3 are currently amended. Claims 9-16 are newly added. No new matter is added. Claim 6 was previously cancelled. As such, claims 1-5 and 7-16 are now pending.

Applicant respectfully requests reconsideration of claims 1-5, 7 and 8 and consideration of claims 9-16 in view of the foregoing amendments and in view of the reasons that follow.

Rejection of Claims 1-5, 7 and 8 Under 35 U.S.C. 103

On page 2 of the Office action, claims 1-5, 7 and 8 were rejected under 35 U.S.C. 103(a) as being unpatentable over Palara ("Palara," US 5,408,124) in view of Odekirk ("Odekirk," US 6,388,272).

Applicant respectfully traverses these rejections in that these claims are patentable over Palara and Odekirk.

Moreover, claim 1 has been amended to further distinguish the claim over the cited references. In more detail, amended claim 1 recites, in relevant portions, a bipolar transistor "wherein the transistor has a specific area resistance less than 500mOhms mm^2 when the metal layer has a thickness less than 3μm" and "wherein the thickness of said metal layer is greater than 3μm. (Emphasis added.)

Support for these features can be found, for example, in page 4, lines 8-17, and in page 5, line 28 to page 6, line 8 of Applicant's specification.

Applicant respectfully submits that neither Palara nor Odekirk, whether individually or in combination, discloses or suggests features of claim 1.

The Examiner acknowledges that Palara "does not teach wherein the transistor has a specific area resistance less than 500mOhms mm^2." (Office Action, page 3.) Because Palara does not teach wherein the transistor has a specific area resistance less than 500mOhms mm^2, Applicant respectfully submits that Palara does not disclose or suggest "wherein the transistor has a specific area resistance less than 500mOhms mm^2 when the metal layer has a thickness less than 3μm[,]" as recited in claim 1. (Emphasis added.) Further, Palara does not disclose or suggest "wherein the thickness of said metal layer is greater than 3μm[,]" as also recited in claim 1. (Emphasis added.)

However, the Examiner contends that Odekirk addresses these features. Applicant respectfully traverses this contention.

In citing Odekirk, the Examiner apparently cites Odekirk's disclosure that "[b]oth [Ni and TiC] exhibit specific contact resistances between $1x10^{-5}$ $\Omega \cdot cm^2$ and $1x10^{-6}$ $\Omega \cdot cm^2$[.]" (Odekirk, col. 2, lines 28-29.)

Applicant respectfully submits that the above disclosure of Odekirk does not disclose or suggest "wherein the transistor has a specific area resistance less than 500mOhms mm^2 when the metal layer has a thickness less than 3μm[,]" as recited in claim 1. (Emphasis added.) Furthermore, the above disclosure of Odekirk does not disclose or suggest "wherein the thickness of said metal layer is greater than 3μm[,]" as also recited in claim 1. (Emphasis added.)

At least for the reasons explained, it is believed that claim 1 is patentable over Palara in view of Odekirk.

Claims 2-5, 7 and 8 depend from claim 1. At least for this reason, claims 2-5, 7 and 8 are patentable over the cited references.

Further, amended claim 2 recites "wherein the thickness of the metal layer is no less than 4μm." (Emphasis added.)

Further, amended claim 3 recites "wherein the thickness of the metal layer is no less than 6μm." (Emphasis added.)

Applicant respectfully submits that these features further distinguish these claims over the cited art.

Regarding claims 2 and 3, the Examiner acknowledges that Palara does not teach the claimed features. (See Office Action, page 3.) However, the Examiner contends that "it would have been obvious to one of ordinary skill to determine the optimum . . . thickness of the metal layer[.]" (Office Action, page 4.) The Examiner further states:

> . . . Note that the specification contains no disclosure of either the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical[.] (Office Action, page 4.)

Applicant respectfully traverses the contention that it would have been obvious to one of ordinary skill in the art to determine the optimum thickness of the metal layer. Moreover, Applicant respectfully submits that the specification of this application contains disclosure of the critical aspects of the ranges in the claimed embodiments.

For example, Applicant's specification provides:

> The thickness of the metal layer defining the base contacts 6 and emitter contacts 7 is chosen in order to help ensure more even biasing of the emitter region 4/base region 3 junction to reduce the parasitic voltage drop across the emitter metal contacts 7. Reducing the voltage drop in the tracks leading to the diverse base region contacts ensures that the voltage bias applied to the emitter/base junction is more evenly distributed, this ensures more even current density across the transistor, reducing the saturation resistance.
>
> The inventors of the present invention have demonstrated that this seemingly simple expedient, when applied to a bipolar transistor already designed to have a low $V_{CE(sat)}$ (i.e. a specific area resistance less than about 500 mOhms.mm^2, can provided further reductions in $V_{CE(sat)}$ of up to around 30%. (Applicant's specification, page 5, line 28 to page 6, line 8.) (Emphasis added.)

Furthermore, Applicant's specification provides:

> A bipolar transistor **not already optimised** for low saturation voltage (i.e. with a specific area resistance greater than about 500 mOhms.mm^2) would show no significant improvement to the saturation voltage by thickening the metal contact in accordance with the present invention since the saturation voltage is affected more by the other parameters described above than by the thickness of the metal contacts. With bipolar transistor designs **already optimised** for low saturation voltage increasing the thickness of the metal contacts further reduces the saturation voltage. This reduction in saturation voltage is progressive and proportional to the thickness of the metal contact and track. Significant improvements to the saturation voltage have been observed with a metal thickness of between 4 μm and 6 μm, with 6 μm, the preferable thickness, reducing the saturation voltage of a bipolar transistor optimised for low saturation performance by a up to a further 30%. (Applicant's specification, page 6, lines 19-30.) (Emphasis added.)

As such, Applicant respectfully submits that the specification of this application does contain disclosure of the critical aspects of the ranges claimed in claims 2 and 3. Therefore, claims 2 and 3 are further patentable over the cited art.

New Claims

New dependent claim 9 depends from claim 1. At least for this reason, claim 9 is patentable over the cited art.

New independent claim 10 recites:

> A method of manufacturing a bipolar transistor, the method comprising:
>
> providing a bipolar transistor including a base region, an emitter region and a metal layer providing contacts to the base region and the emitter region, the bipolar transistor having a specific area resistance of less than 500mOhms mm^2 when the metal layer has a thickness of less than 3μm; and
>
> increasing the thickness of the metal layer to be greater than 3μm. (Emphasis added.)

Support for features of claim 10 can be found, for example, in page 3, line 25 to page 4, line 17 of Applicant's specification.

For reasons similar to those explained above with respect to claim 1, Applicant respectfully submits that claim 10 is patentable over the cited references.

New dependent claims 11-16 recite features similar to those recited in claims 2-5, 7 and 8, respectively. New dependent claims 11-16 depend from claim 10. At least for this reason, Applicant respectfully submits that new claims 11-16 are patentable over the cited references.

Further, as previously noted, claims 11 and 12 recite features similar to those recited in claims 2 and 3, respectively. For reasons similar to those explained above with respect to claims 2 and 3, Applicant respectfully submits that claims 11 and 12 are patentable over the cited references.

Concluding Remarks

Applicant believes that the present application is now in condition for allowance. Favorable reconsideration of the application as amended is respectfully requested.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 19-0741. Should no proper payment be enclosed herewith, as by the credit card payment instructions in EFS-Web being incorrect or absent, resulting in a rejected or incorrect credit card transaction, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 19-0741. If any extensions of time are needed for timely acceptance of papers submitted herewith, Applicant hereby petitions for such extension under 37 C.F.R. §1.136 and authorizes payment of any such extensions fees to Deposit Account No. 19-0741.

Respectfully submitted,

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